NUP2114UCMR6

Transient Voltage Suppressors

Low Capacitance ESD Protection for High Speed Data

The NUP2114UCMR6 transient voltage suppressor is designed to protect high speed data lines from ESD. Ultra−low capacitance and high level of ESD protection makes this device well suited for use in USB 2.0 high speed applications.

Features

- Low Capacitance 0.8 pF
- Low Clamping Voltage
- Stand Off Voltage: 5 V
- Low Leakage
- ESD Rating of Class 3B (Exceeding 8 kV) per Human Body model and Class C (Exceeding 400 V) per Machine Model
- IEC61000−4−2 Level 4
- UL Flammability Rating of 94 V−0
- This is a Pb−Free Device

Typical Applications

- High Speed Communication Line Protection
- USB 2.0 High Speed Data Line and Power Line Protection
- Gigabit Ethernet
- Notebook Computers

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Seconds)	T_L	260	°C
Human Body Model (HBM) Machine Model (MM) IEC61000−4−2 Contact IEC61000−4−2 Air	ESD	16000 400 13000 15000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

See Application Note AND8308/D for further description of survivability specs.

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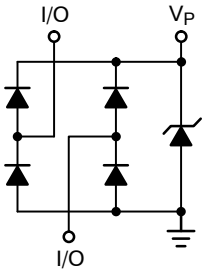
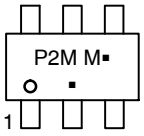


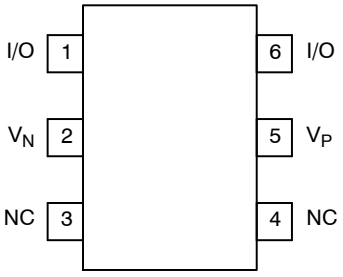
TSOP−6
CASE 318G

MARKING DIAGRAM



P2M = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping
NUP2114UCMR6T1G	TSOP−6 (Pb−Free)	3000 / Tape & Reel

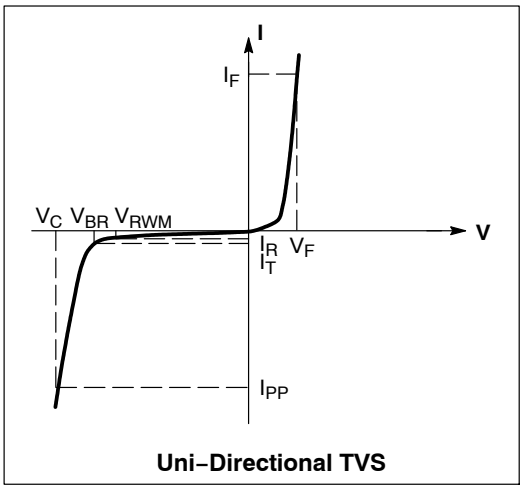
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F
P_{pk}	Peak Power Dissipation
C	Max. Capacitance @ V_R = 0 and f = 1.0 MHz

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



Uni−Directional TVS

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	(Note 1)			5.0	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, (Note 2)	6.0	7.5		V
Reverse Leakage Current	I_R	V_{RWM} = 5 V			1.0	μA
Clamping Voltage	V_C	I_{PP} = 5 A (Note 3)		9.0		V
Clamping Voltage	V_C	I_{PP} = 8 A (Note 3)		10		V
Maximum Peak Pulse Current	I_{PP}	8x20 μs Waveform			12	A
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins and GND		0.8	1.0	pF
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins			0.5	pF
Clamping Voltage	V_C	@ I_{PP} = 1 A (Note 4)			12	V
Clamping Voltage	V_C	Per IEC 61000−4−2 (Note 5)	Figures 1 and 2			V

1. TVS devices are normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal or greater than the DC or continuous peak operating voltage level.
2. V_{BR} is measured at pulse test current I_T.
3. Nonrepetitive current pulse (Pin 5 to Pin 2)
4. Surge current waveform per Figure 5.
5. Typical waveform. For test procedure see Figures 3 and 4 and Application Note AND8307/D.

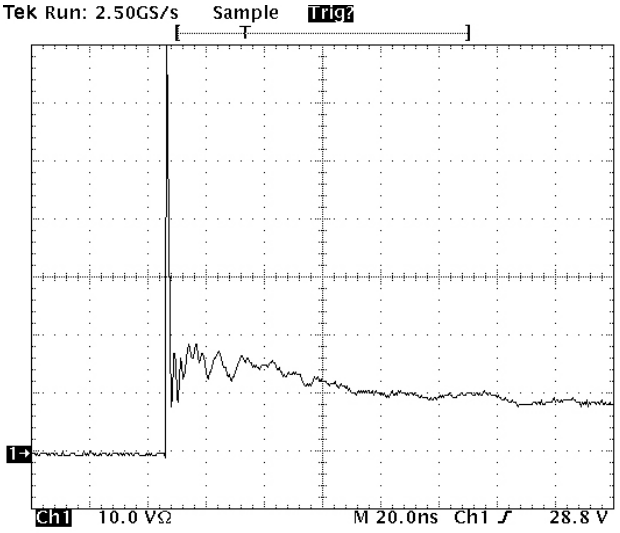


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2

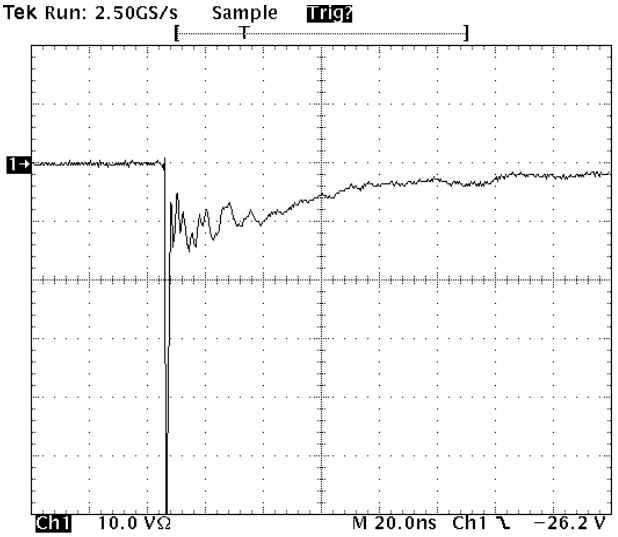


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

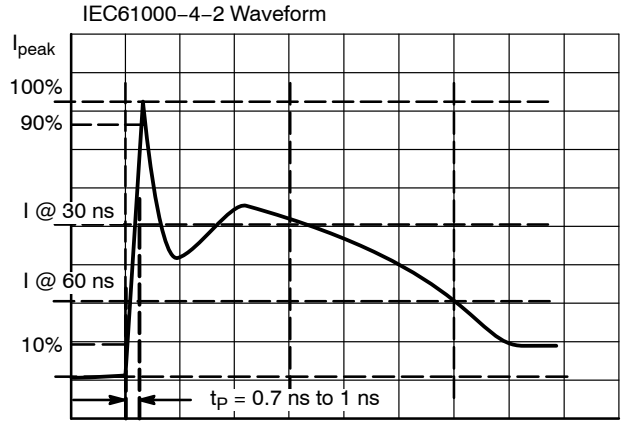


Figure 3. IEC61000−4−2 Spec

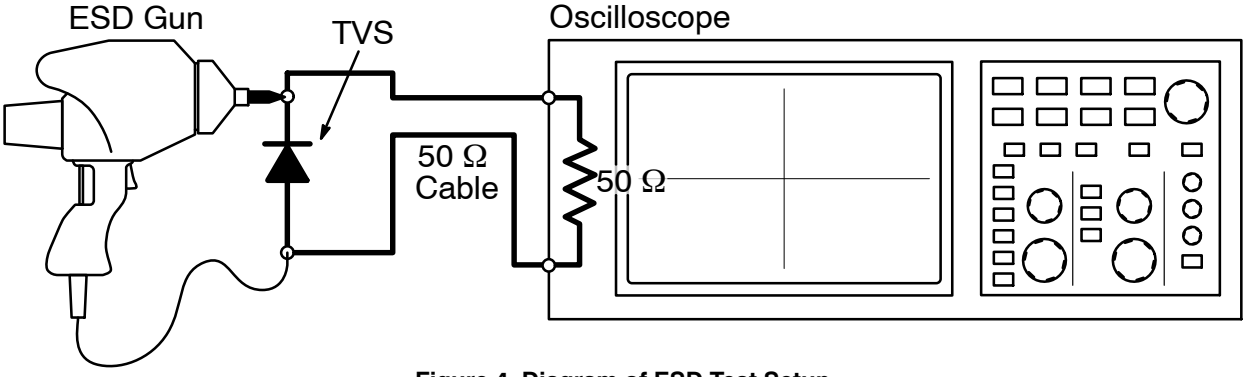


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

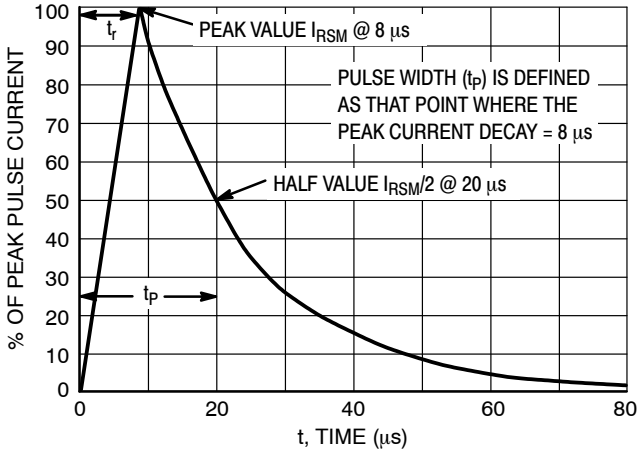


Figure 5. 8 X 20 μs Pulse Waveform

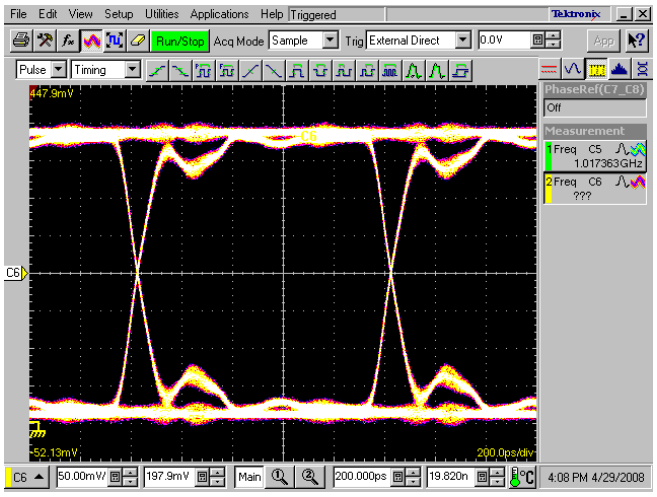
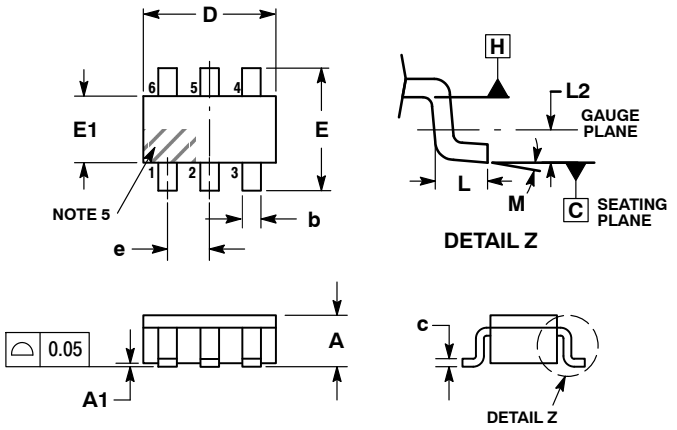


Figure 6. 500 MHz Data Pattern

PACKAGE DIMENSIONS

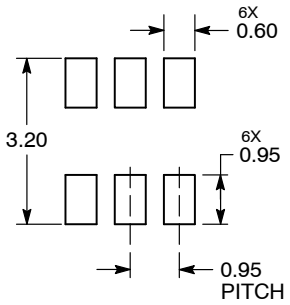
TSOP−6
CASE 318G−02
ISSUE U



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	–	10°

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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